# DATA SHEET

# TDA8760
## 10-bit high-speed analog-to-digital converter

Product specification
Supersedes data of April 1994
File under Integrated Circuits, IC02

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Philips
Semiconductors

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# 10-bit high-speed analog-to-digital converter

# TDA8760

## FEATURES

- 10-bit resolution
- Sampling rate up to 40 MHz
- Total Harmonic Distortion (THD): –65 dB at 4.43 MHz full-scale and a 40 MHz clock frequency
- High signal-to-noise ratio over a large analog input frequency range (8.8 effective bits at 10 MHz full-scale input at a 40 MHz clock frequency)
- +5 V power supplies
- Binary or two's complement 3-state TTL outputs
- In-range 3-state TTL output
- TTL compatible digital inputs
- LOW-level AC clock input signal allowed
- Power dissipation 850 mW (typical)
- Low analog input capacitance (typ. 4.5 pF), no buffer amplifier required
- No external sample-and-hold circuit required
- Analog Input; single or differential
- External amplitude range control
- Voltage controlled regulator included.

## APPLICATIONS

- High-speed analog-to-digital conversion for
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Digital video broadcasting (satellite and cable)
  - Transient signal analysis
  - High energy physics research
  - Sigma-delta (SD) modulators
  - Medical imaging
  - Radar pulse digitizing.

## GENERAL DESCRIPTION

The TDA8760 is a monolithic bipolar 10-bit Analog-to-Digital Converter (ADC) for video or other applications. It converts the analog input signal into 10-bit binary coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible. However, a sine wave clock input signal is allowed.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO}$ | output supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{CCA}$ | analog supply current | | – | 95 | 100 | mA |
| $I_{CCD}$ | digital supply current | | – | 40 | 45 | mA |
| $I_{CCO}$ | output supply current | | – | 35 | 40 | mA |
| ILE | DC integral linearity error | $f_{clk}$ = 4 MHz | – | ±1.0 | ±2.0 | LSB |
| DLE | DC differential linearity error | $f_{clk}$ = 4 MHz | – | ±0.6 | ±1.0 | LSB |
| AILE | AC integral linearity error | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | ±1.2 | ±2.0 | LSB |
| $f_{clk(max)}$ | maximum clock frequency | | | | | |
| | TDA8760K/2 | | 20 | – | – | MHz |
| | TDA8760K/4 | | 40 | – | – | MHz |
| $P_{tot}$ | total power dissipation | | – | 850 | 970 | mW |
| $T_{amb}$ | operating ambient temperature | | 0 | – | +70 | °C |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | SAMPLING FREQUENCY (MHz) |
|---|---|---|---|---|
| | NAME | DESCRIPTION | VERSION | |
| TDA8760K/2 | PLCC44 | plastic leaded chip carrier; 44 leads | SOT187-2 | 20 |
| TDA8760K/4 | | | | 40 |

## BLOCK DIAGRAM

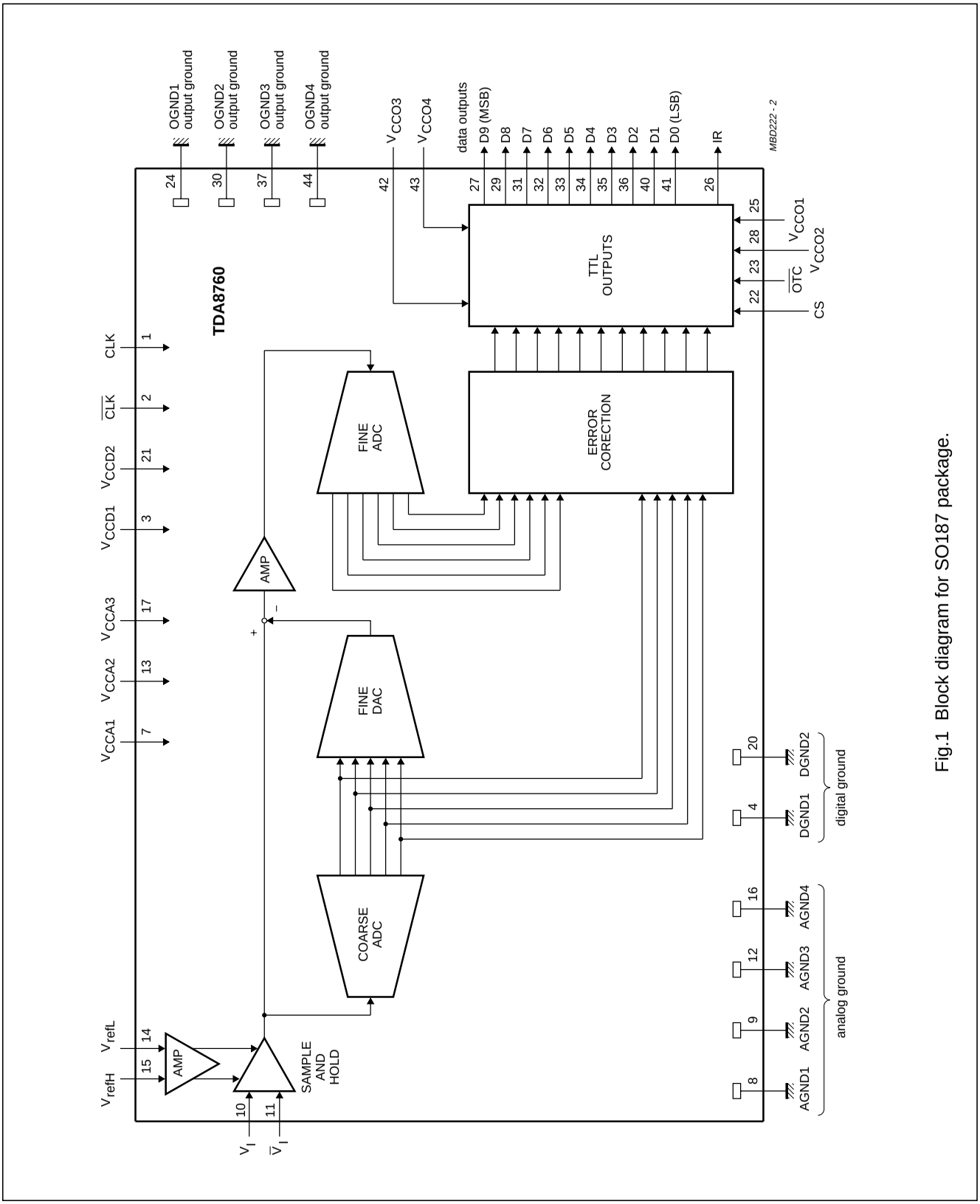



Fig.1 Block diagram for SO187 package.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| CLK | 1 | clock input |
| $\overline{CLK}$ | 2 | complementary clock input |
| $V_{CCD1}$ | 3 | digital supply voltage (+5 V) |
| DGND1 | 4 | digital ground |
| n.c. | 5 | not connected |
| n.c. | 6 | not connected |
| $V_{CCA1}$ | 7 | analog supply voltage (+5 V) |
| AGND1 | 8 | analog ground |
| AGND2 | 9 | analog ground |
| $V_I$ | 10 | analog input voltage |
| $\overline{V_I}$ | 11 | complementary analog input voltage |
| AGND3 | 12 | analog ground |
| $V_{CCA2}$ | 13 | analog supply voltage (+5 V) |
| $V_{refL}$ | 14 | reference voltage LOW |
| $V_{refH}$ | 15 | reference voltage HIGH |
| AGND4 | 16 | analog ground |
| $V_{CCA3}$ | 17 | analog supply voltage (+5 V) |
| n.c. | 18 | not connected |
| n.c. | 19 | not connected |
| DGND2 | 20 | digital ground |
| $V_{CCD2}$ | 21 | digital supply voltage (+5 V) |
| CS | 22 | chip select input (TTL level input; active HIGH) |
| $\overline{OTC}$ | 23 | output two’s complement |
| OGND1 | 24 | output ground |
| $V_{CCO1}$ | 25 | output supply voltage (+5 V) |
| IR | 26 | in-range output |
| D9 | 27 | data output, bit 9 (MSB) |
| $V_{CCO2}$ | 28 | output supply voltage (+5 V) |
| D8 | 29 | data output, bit 8 |
| OGND2 | 30 | output ground |
| D7 | 31 | data output, bit 7 |
| D6 | 32 | data output, bit 6 |
| D5 | 33 | data output, bit 5 |
| D4 | 34 | data output, bit 4 |
| D3 | 35 | data output, bit 3 |
| D2 | 36 | data output, bit 2 |
| OGND3 | 37 | output ground |
| n.c. | 38 | not connected |
| n.c. | 39 | not connected |
| D1 | 40 | data output, bit 1 |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| D0 | 41 | data output, bit 0 (LSB) |
| $V_{CCO3}$ | 42 | output supply voltage (+5 V) |
| $V_{CCO4}$ | 43 | output supply voltage (+5 V) |
| OGND4 | 44 | output ground |

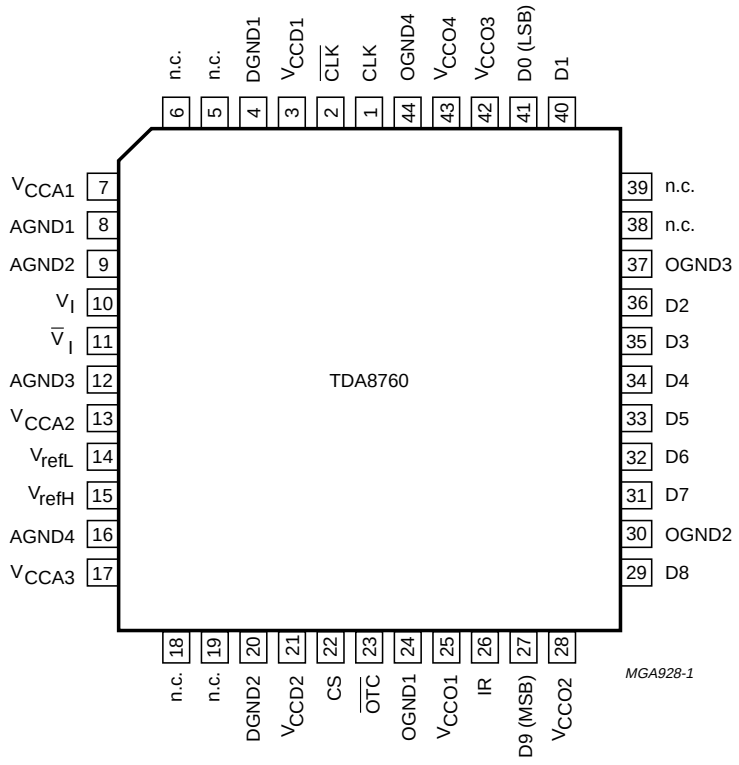



Fig.2 Pin configuration for SOT187-2.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | | –0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage | | –0.3 | +7.0 | V |
| $V_{CCO}$ | output supply voltage | | –0.3 | +7.0 | V |
| $\Delta V_{CC1}$ | supply voltage difference between $V_{CCA}$ and $V_{CCD}$ | | –0.5 | +0.5 | V |
| $\Delta V_{CC2}$ | supply voltage difference between $V_{CCO}$ and $V_{CCD}$ | | –0.5 | +0.5 | V |
| $\Delta V_{CC3}$ | supply voltage difference between $V_{CCA}$ and $V_{CCO}$ | | –0.5 | 0.5 | V |
| $V_I$ | input voltage | referenced to AGND | 0.3 | $V_{CCA}$ | V |
| $V_{I(p-p)}$ | input voltage for differential clock drive (peak-to-peak value) | | – | $V_{CCD}$ | V |
| $I_O$ | output current | | – | 10 | mA |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | 0 | +70 | °C |
| $T_j$ | junction temperature | | – | +150 | °C |

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|---|---|---|
| $R_{th\ j\text{-}a}$ | Thermal resistance from junction to ambient in free air | |
| | TDA8760K/4 | 35 K/W |
| | TDA8760K/2 | 46 K/W |

## CHARACTERISTICS

$V_{CCA} = V_{CCD} = V_{CCO}$ = 4.75 to 5.25 V; AGND and DGND shorted together;
$V_{CCA} - V_{CCD} = V_{CCO} - V_{CCD} = V_{CCA} - V_{CCO}$ = –0.25 to +0.25 V; $T_{amb}$ = 0 to +70 °C; unless otherwise specified.
Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; $T_{amb}$ = 25 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA}$ | analog supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCD}$ | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCO}$ | output supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{CCA}$ | analog supply current | | – | 95 | 100 | mA |
| $I_{CCD}$ | digital supply current | | – | 40 | 45 | mA |
| $I_{CCO}$ | output supply current | all outputs LOW | – | 35 | 40 | mA |
| **Inputs** | | | | | | |
| CLK AND $\overline{\text{CLK}}$ (REFERENCED TO DGND); note 1 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{clk}$ or $V_{\overline{clk}}$ = 0.4 V | –400 | – | – | mA |
| $I_{IH}$ | HIGH level input current | $V_{clk}$ or $V_{\overline{clk}}$ = 2.0 V | – | – | 100 | mA |
| | | $V_{clk}$ or $V_{\overline{clk}} = V_{CCD}$ | – | – | 300 | mA |
| $Z_I$ | input impedance | $f_{clk}$ = 40 MHz | – | 2 | – | kΩ |
| $C_I$ | input capacitance | $f_{clk}$ = 40 MHz | – | 4.5 | – | pF |
| $\Delta V_{clk}$ | AC input voltage for switching ($V_{clk} - V_{\overline{clk}}$) | DC level = 1.5 V | 0.5 | – | 2.0 | V |
| | | DC level = 2.5 V | 1.5 | – | 5.0 | V |
| $\overline{\text{OTC}}$ AND CS (REFERENCED TO DGND); see Table 3 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{IL}$ = 0.8 V | –400 | – | – | μA |
| $I_{IH}$ | HIGH level input current | $V_{IH}$ = 2.0 V | – | – | 20 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_I$ AND $\overline{V}_I$ (REFERENCED TO AGND); see also Tables 1 and 2 | | | | | | |
| $I_{IL}$ | LOW level input current | $V_{refH} - V_{refL}$ = 1.5 V | – | 7 | – | μA |
| $I_{IH}$ | HIGH level input current | $V_{refH} - V_{refL}$ = 1.5 V | – | 22 | – | μA |
| $Z_I$ | input impedance | $f_i$ = 4.43 MHz | – | 2 | – | kΩ |
| $C_I$ | input capacitance | $f_i$ = 4.43 MHz | – | 4.5 | – | pF |
| $V_{Ioffset(d)}$ | input offset voltage | differential mode; $V_I = \overline{V}_I$; output code 511; Table 1 | | | | |
| | | $V_{CCA}$ = 5 V | 3.3 | 3.4 | 3.6 | V |
| | | $V_{CCA}$ = 4.75 V | 3.2 | – | 3.45 | V |
| | | $V_{CCA}$ = 5.25 V | 3.3 | – | 3.8 | V |
| $V_{Ioffset(s)}$ | input offset voltage | single mode; $V_I = V_{Ioffset(s)}$; output code 511; Table 2 | | | | |
| | | $V_{CCA}$ = 5 V | 3.6 | 3.7 | 3.8 | V |
| | | $V_{CCA}$ = 4.75 V | 3.5 | – | 3.65 | V |
| | | $V_{CCA}$ = 5.25 V | 3.6 | – | 4.0 | V |
| **Voltage controlled regulator inputs $V_{refH}$ and $V_{refL}$ (referenced to AGND); differential input** | | | | | | |
| $V_{refH}$ | reference voltage HIGH | | 4.0 | 4.5 | $V_{CCA}$ | V |
| $V_{refL}$ | reference voltage LOW | | 2.5 | 3.0 | 3.5 | V |
| $V_{I(p-p)}$ | input voltage amplitude (peak-to-peak value) | | 1.4 | 1.5 | 1.6 | V |
| $I_{refH}$ | input current at $V_{refH}$ | | – | 10 | – | μA |
| $I_{refL}$ | input current at $V_{refL}$ | | – | 10 | – | μA |
| **Voltage controlled regulator inputs $V_{refH}$ and $V_{refL}$ (referenced to AGND); single input** | | | | | | |
| $V_{refH}$ | reference voltage HIGH | | 4.0 | 4.4 | $V_{CCA}$ | V |
| $V_{refL}$ | reference voltage LOW | | 2.5 | 3.0 | 3.5 | V |
| $V_{I(p-p)}$ | input voltage amplitude (peak-to-peak value) | | 1.3 | 1.4 | 1.5 | V |
| $I_{refH}$ | input current at $V_{refH}$ | | – | 10 | – | μA |
| $I_{refL}$ | input current at $V_{refL}$ | | – | 10 | – | μA |
| **Outputs (referenced to DGND)** | | | | | | |
| DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO DGND) | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_O$ = 2 mA | 0 | – | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_O$ = –0.4 mA | 2.4 | – | $V_{CCD}$ | V |
| $I_O$ | output current in 3-state mode | 0.4 V < $V_O$ < $V_{CCO}$ | –20 | – | +20 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Switching characteristics** | | | | | | |
| CLOCK FREQUENCY $f_{clk}$ (note 1; see Fig.3) | | | | | | |
| $f_{clk(min)}$ | minimum clock frequency | | – | – | 1 | MHz |
| $f_{clk(max)}$ | maximum clock frequency | | | | | |
| | TDA8760K/4 | | 40 | – | – | MHz |
| | TDA8760K/2 | | 20 | – | – | MHz |
| $t_{CPH}$ | clock pulse width HIGH | note 7 | 10 | – | – | ns |
| $t_{CPL}$ | clock pulse width LOW | | 8 | – | – | ns |
| **Analog signal processing in differential input mode;** see Table 1**; 50% clock duty factor; $V_{I(p-p)} = V_{refH} - V_{refL} = 1.5$ V** | | | | | | |
| LINEARITY | | | | | | |
| ILE | DC integral linearity error | $f_{clk}$ = 4 MHz | – | ±1.0 | ±2.0 | LSB |
| DLE | DC differential linearity error | $f_{clk}$ = 4 MHz | – | ±0.6 | ±1.0 | LSB |
| AILE | AC integral linearity error | note 3 | – | ±1.2 | ±2.0 | LSB |
| OFE | offset error | $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $V_I = \overline{V_I}$; $T_{amb} = 25$ °C; output code = 511 | –3 | – | +3 | LSB |
| GE | gain error; amplitude spread between devices | $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; $V_{refH} - V_{refL} = 1.5$ V | –10 | – | +10 | LSB |
| BANDWIDTH ($f_{clk}$ = 40 MHz); note 9 | | | | | | |
| B | Analog bandwidth | –1 dB | – | 140 | – | MHz |
| | | –3 dB | – | 220 | – | MHz |
| HARMONICS ($f_{clk}$ = 40 MHz); see Figs 6, 8 and 9 | | | | | | |
| $f_1$ | fundamental harmonics (full scale) | $f_i$ = 4.43 MHz | – | – | 0 | dB |
| $f_{all}$ | harmonics (full scale); all components | $f_i$ = 4.43 MHz | | | | |
| | second harmonics | | – | –70 | –63 | dB |
| | third harmonics | | – | –70 | –63 | dB |
| THD | total harmonic distortion | $f_i$ = 4.43 MHz; note 2 | – | –65 | –60 | dB |
| SIGNAL-TO-NOISE RATIO; notes 4 and 5; see Figs 6, 8 and 9 | | | | | | |
| SNR | signal-to-noise ratio | without harmonics; $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz; $T_{amb} = 25$ °C | 54 | 56 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| EFFECTIVE BITS; notes 4 and 5; see Figs 6, 8 and 9 | | | | | | |
| EB | effective bits TDA8760K/2 ($f_{clk}$ = 20 MHz) | $f_i$ = 4.43 MHz | – | 8.90 | – | bits |
| | | $f_i$ = 7.5 MHz | – | 8.70 | – | bits |
| | effective bits TDA8760K/4 ($f_{clk}$ = 40 MHz) | $f_i$ = 4.43 MHz | – | 8.80 | – | bits |
| | | $f_i$ = 10 MHz | – | 8.80 | – | bits |
| | | $f_i$ = 15 MHz | – | 8.70 | – | bits |
| TWO-TONE | | | | | | |
| Two-tone | two-tone intermodulation rejection | $f_{clk}$ = 40 MHz; note 8 | – | –65 | – | dB |
| BIT ERROR RATE | | | | | | |
| BER | bit error rate | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz; $V_I$ = ±16 LSB at code 512 | – | $2 \times 10^{-12}$ | – | times/ samples |
| DIFFERENTIAL GAIN; SEE Fig.5 | | | | | | |
| $G_{diff}$ | differential gain | $f_{clk}$ = 20 MHz; $f_i$ = 4.43 MHz | – | 0.5 | – | % |
| | | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | 1.0 | – | % |
| DIFFERENTIAL PHASE | | | | | | |
| $\Phi_{diff}$ | differential phase | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | 0.1 | 0.2 | deg |
| **Analog signal processing in single input mode;** see Table 2**; 50% clock duty factor; $V_{I(p-p)} = V_{refH} - V_{refL}$ = 1.4 V** | | | | | | |
| LINEARITY | | | | | | |
| ILE | DC integral linearity error | $f_{clk}$ = 4 MHz | – | ±1.0 | ±2.0 | LSB |
| DLE | DC differential linearity error | $f_{clk}$ = 4 MHz | – | ±0.6 | ±1.0 | LSB |
| AILE | AC integral linearity error | note 3 | – | ±1.2 | ±2.0 | LSB |
| BANDWIDTH ($f_{clk}$ = 40 MHz); note 9 | | | | | | |
| B | Analog bandwidth | –1 dB | – | 140 | – | MHz |
| | | –3 dB | – | 220 | – | MHz |
| HARMONICS ($f_{clk}$ = 40 MHz); see Fig.7 | | | | | | |
| $f_1$ | fundamental harmonics (full scale) | $f_i$ = 4.43 MHz | – | – | 0 | dB |
| $f_{all}$ | harmonics (full scale); all components | $f_i$ = 4.43 MHz | | | | |
| | second harmonics | | – | –61 | – | dB |
| | third harmonics | | – | –62 | – | dB |
| THD | total harmonic distortion | $f_i$ = 4.43 MHz; note 2 | – | –59 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| SIGNAL-TO-NOISE RATIO; notes 4 and 5; see Fig.7 | | | | | | |
| SNR | signal-to-noise ratio | without harmonics; $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz; $T_{amb}$ = 25 °C | 54 | 56 | – | dB |
| EFFECTIVE BITS; notes 4 and 5; see Fig.7 | | | | | | |
| EB | effective bits TDA8760K/2 ($f_{clk}$ = 20 MHz) | $f_i$ = 4.43 MHz | – | 8.70 | – | bits |
| | | $f_i$ = 7.5 MHz | – | 8.50 | – | bits |
| | effective bits TDA8760K/4 ($f_{clk}$ = 40 MHz) | $f_i$ = 4.43 MHz | – | 8.50 | – | bits |
| | | $f_i$ = 10 MHz | – | 8.20 | – | bits |
| TWO-TONE | | | | | | |
| Two-tone | two-tone intermodulation rejection | $f_{clk}$ = 40 MHz; note 8 | – | –60 | – | dB |
| BIT ERROR RATE | | | | | | |
| BER | bit error rate | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz; $V_I$ = ±16 LSB at code 512 | – | $2 \times 10^{-12}$ | – | times/ samples |
| DIFFERENTIAL GAIN; see Fig.5 | | | | | | |
| $G_{diff}$ | differential gain | $f_{clk}$ = 20 MHz; $f_i$ = 4.43 MHz | – | 0.5 | – | % |
| | | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | 1.0 | – | % |
| DIFFERENTIAL PHASE | | | | | | |
| $\Phi_{diff}$ | differential phase | $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | 0.1 | 0.2 | deg |
| **Timing** (note 6; see Fig.3; **CL = 15 pF**) | | | | | | |
| $t_{ds}$ | sampling delay time | | – | – | 2 | ns |
| $t_h$ | output hold time | | 8 | – | – | ns |
| $t_d$ | output delay time | | – | 12 | 16 | ns |
| **3-state output delay times** (see Fig.4) | | | | | | |
| $t_{dZH}$ | enable HIGH | | – | 12 | 16 | ns |
| $t_{dZL}$ | enable LOW | | – | 12 | 16 | ns |
| $t_{dHZ}$ | disable HIGH | | – | 8 | 12 | ns |
| $t_{dLZ}$ | disable LOW | | – | 16 | 20 | ns |

**Notes**

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. There are three modes of operation:
   a) TTL mode 1:
   CLK input is at TTL level with a threshold voltage of 1.5 V and sampling is taken on the falling edge of the clock input signal. $\overline{CLK}$ decoupled to DGND via a 100 nF capacitor.
   b) TTL mode 2:
   $\overline{CLK}$ input is at TTL level with threshold voltage of 1.5 V and sampling is taken on the rising edge of the clock input signal. CLK decoupled to DGND via a 100 nF capacitor.
   c) TTL mode 3:
   CLK and $\overline{CLK}$ inputs are at differential TTL levels.
   d) AC driving modes:
   When driving the CLK input directly and with any AC signal of minimum 0.5 V (p-p) and with a DC level of 1.5 V, the sampling takes place at the falling edge of the clock signal.
   When driving the $\overline{CLK}$ input with the same signal, sampling takes place at the rising edge of the clock signal.It is recommended to decouple the $\overline{CLK}$ or CLK input to DGND via a 100 nF capacitor.
2. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:
   a) $$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$
   b) F being the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
3. AC linearity: full-scale differential sine wave ($f_i$ = 4.43 MHz; $f_{clk}$ = 40 MHz).
4. Effective bits with differential input and single input are respectively executed with full scale differential input and full-scale single sine wave.
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR = EB $\times$ 6.02 + 1.76 dB.
6. Output data acquisition: the output data is available after the maximum delay of $t_d$.
7. $t_{CPH}$ of 9 ns (minimum) can be applied at the penalty of 0.5 effective bit drop compared to typical values.
8. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.
9. The –3 dB (or –1 dB) analog bandwidth is determined by the 3 dB (or 1 dB) reduction in the reconstructed output, the input being a full-scale sine wave.

**Table 1** Output coding with differential inputs (typical values to AGND); $V_{I(p-p)} = V_{refH} - V_{refL} = 1.5$ V

| CODE | $V_{I(p-p)}$ | $\overline{V}_{I(p-p)}$ | IR | BINARY OUTPUTS | TWO'S COMPLEMENT OUTPUTS |
|---|---|---|---|---|---|
| | | | | D9 TO D0 | D9 TO D0 |
| underflow | <3.025 | >3.775 | 0 | 0 0 0 0 0 0 0 0 0 0 | 1 0 0 0 0 0 0 0 0 0 |
| 0 | 3.025 | 3.775 | 1 | 0 0 0 0 0 0 0 0 0 0 | 1 0 0 0 0 0 0 0 0 0 |
| 1 | – | – | 1 | 0 0 0 0 0 0 0 0 0 1 | 1 0 0 0 0 0 0 0 0 1 |
| • | – | – | • | • • • • • • • • • • | • • • • • • • • • • |
| 511 | 3.40 | 3.40 | 1 | 0 1 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 1 1 |
| • | – | – | • | • • • • • • • • • • | • • • • • • • • • • |
| 1022 | – | – | 1 | 1 1 1 1 1 1 1 1 1 0 | 0 1 1 1 1 1 1 1 1 0 |
| 1023 | 3.775 | 3.025 | 1 | 1 1 1 1 1 1 1 1 1 1 | 0 1 1 1 1 1 1 1 1 1 |
| overflow | >3.775 | <3.025 | 0 | 1 1 1 1 1 1 1 1 1 1 | 0 1 1 1 1 1 1 1 1 1 |

**Table 2** Output coding with single inputs (typical values to AGND); $V_{I(p-p)} = V_{refH} - V_{refL} = 1.4$ V; $\overline{V}_{I(p-p)} = 3.7$ V

| CODE | $V_{I(p-p)}$ | IR | BINARY OUTPUTS | TWO'S COMPLEMENT OUTPUTS |
|---|---|---|---|---|
| | | | D9 TO D0 | D9 TO D0 |
| underflow | <3.0 | 0 | 0 0 0 0 0 0 0 0 0 0 | 1 0 0 0 0 0 0 0 0 0 |
| 0 | 3.0 | 1 | 0 0 0 0 0 0 0 0 0 0 | 1 0 0 0 0 0 0 0 0 0 |
| 1 | – | 1 | 0 0 0 0 0 0 0 0 0 1 | 1 0 0 0 0 0 0 0 0 1 |
| • | – | • | • • • • • • • • • • | • • • • • • • • • • |
| 511 | 3.7 | 1 | 0 1 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 1 1 |
| • | – | • | • • • • • • • • • • | • • • • • • • • • • |
| 1022 | – | 1 | 1 1 1 1 1 1 1 1 1 0 | 0 1 1 1 1 1 1 1 1 0 |
| 1023 | 4.4 | 1 | 1 1 1 1 1 1 1 1 1 1 | 0 1 1 1 1 1 1 1 1 1 |
| overflow | >4.4 | 0 | 1 1 1 1 1 1 1 1 1 1 | 0 1 1 1 1 1 1 1 1 1 |

**Table 3** Mode selection.

| $\overline{OTC}$ | CS | D0 TO D9 AND IR |
|---|---|---|
| 1 | 1 | binary; active |
| 0 | 1 | two's complement; active |
| X[1] | 0 | high impedance |

**Note**

1. Where: X = don't care.

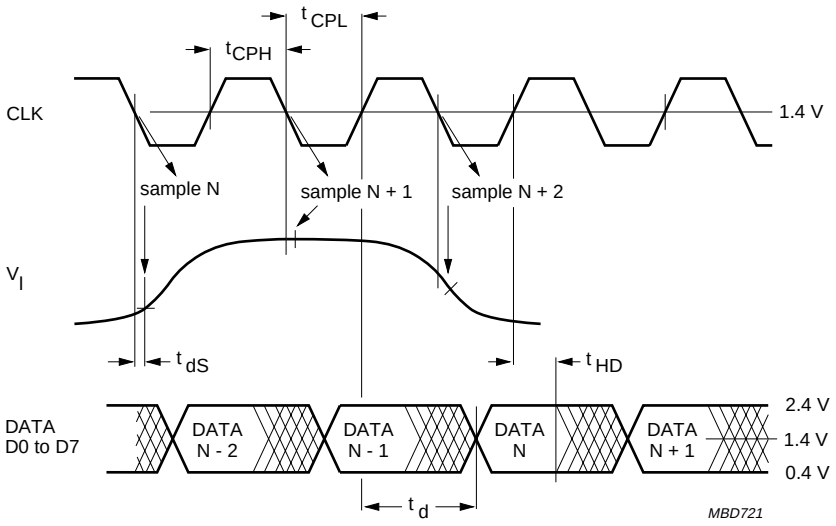
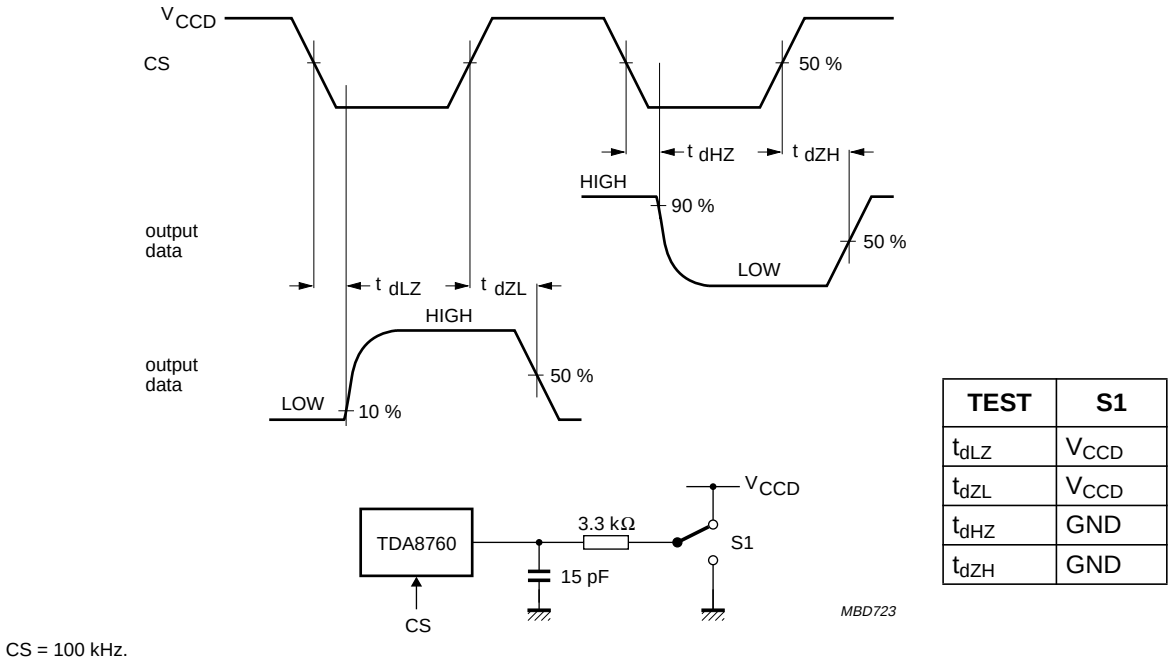


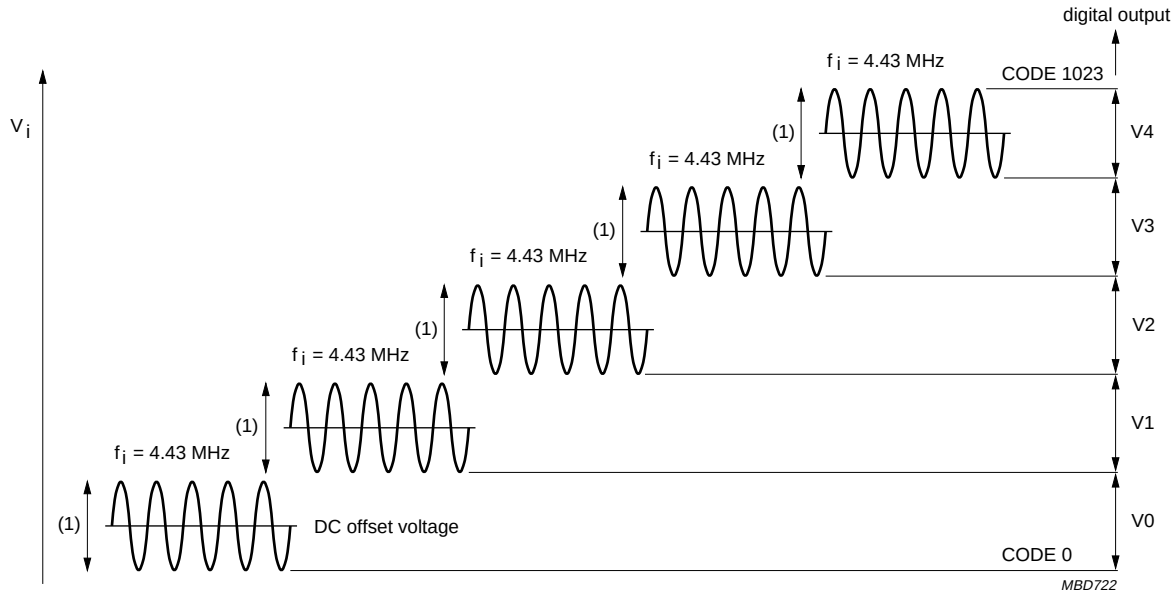

Fig.3 Timing diagram.




| TEST | S1 |
|---|---|
| $t_{dLZ}$ | $V_{CCD}$ |
| $t_{dZL}$ | $V_{CCD}$ |
| $t_{dHZ}$ | GND |
| $t_{dZH}$ | GND |

CS = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.




(1) Full-scale divided-by-5.

$$G_{diff} = \text{maximum of } \left( \frac{V_n(1 \text{ to } 4) - V0}{V0} \right) \times 100\%$$

Fig.5 Differential gain measurement conditions.

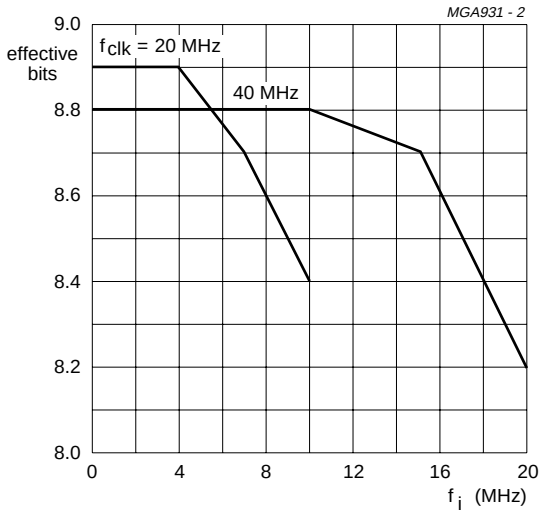



Fig.6 Typical effective bits under differential input mode as a function of input signal frequency.

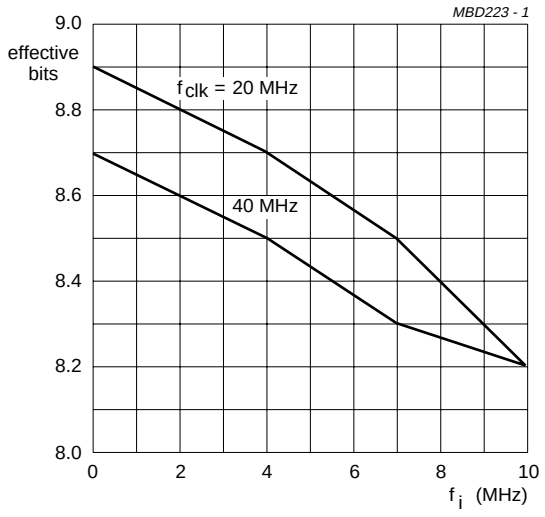
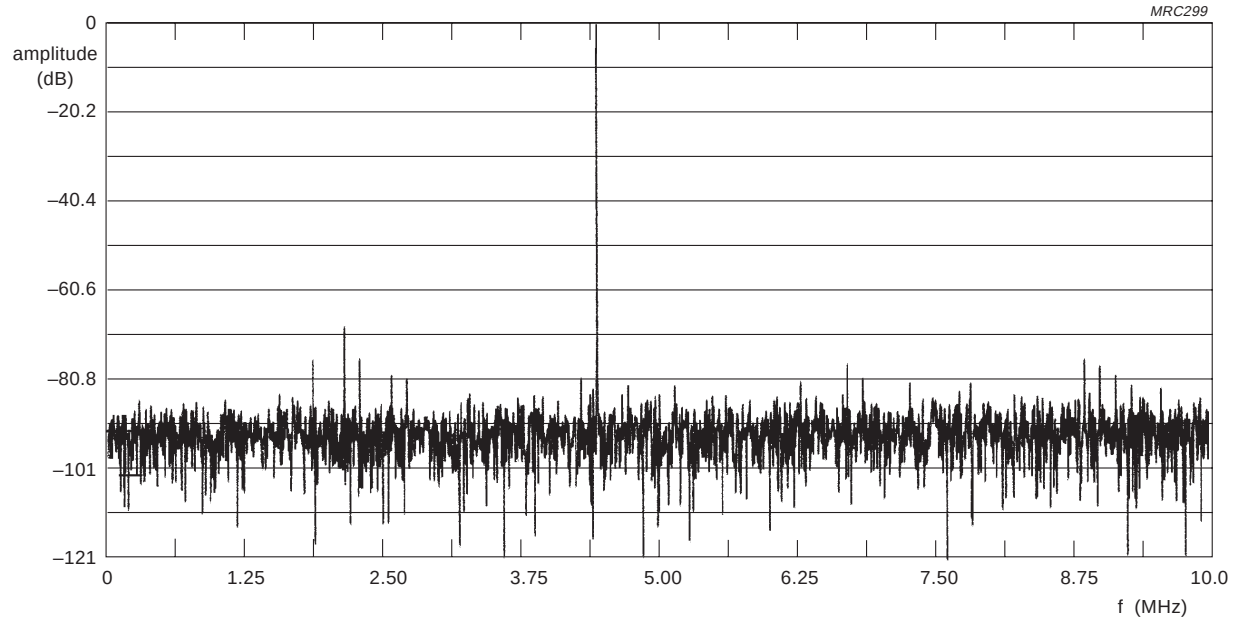
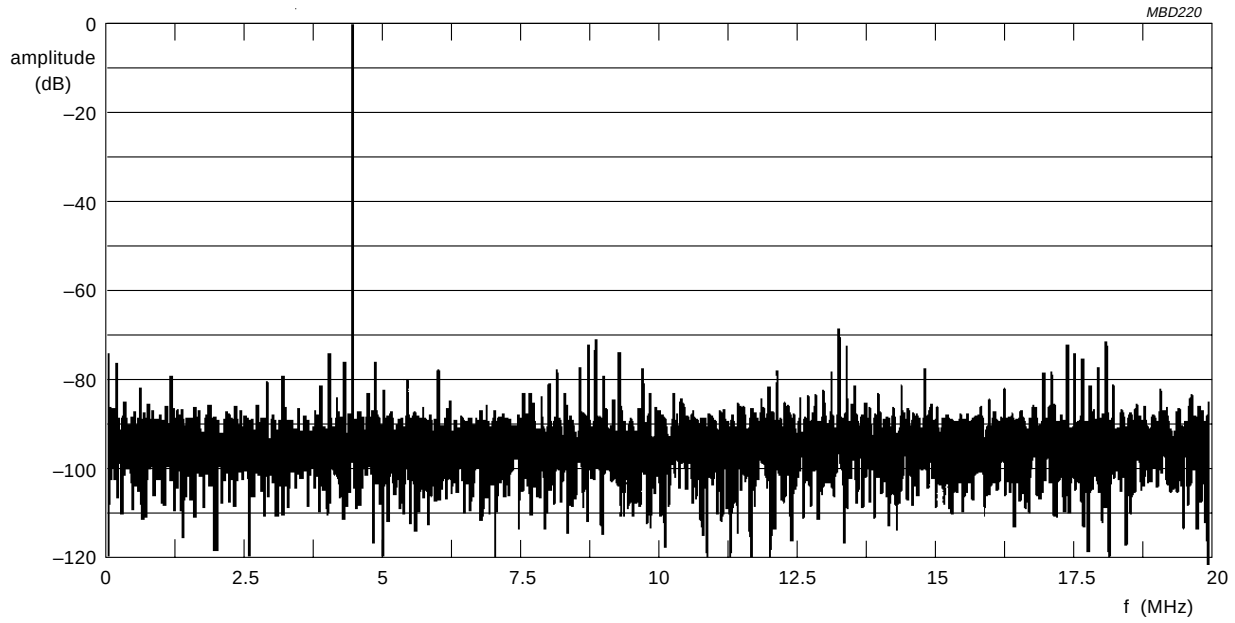



Fig.7 Typical effective bits under single input mode as a function of input signal frequency.




Effective bits: 9.1; THD = –65.81 dB;
Harmonic levels (dB): 2nd = –75.54; 3rd = –76.29; 4th = –74.90; 5th = –67.50; 6th = –90.87.

Fig.8 Fast Fourier Transformer ($f_{clk}$ = 20 MHz; $f_i$ = 4.43 MHz); for differential input mode.




Effective bits: 8.92; THD = –65.86 dB;
Harmonic levels (dB): 2nd = –70.92; 3rd = –68.48; 4th = –75.32; 5th = – 81.40; 6th = –72.69.

Fig.9 Fast Fourier Transformer ($f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz); for differential input mode.

**INTERNAL PIN CONFIGURATION**

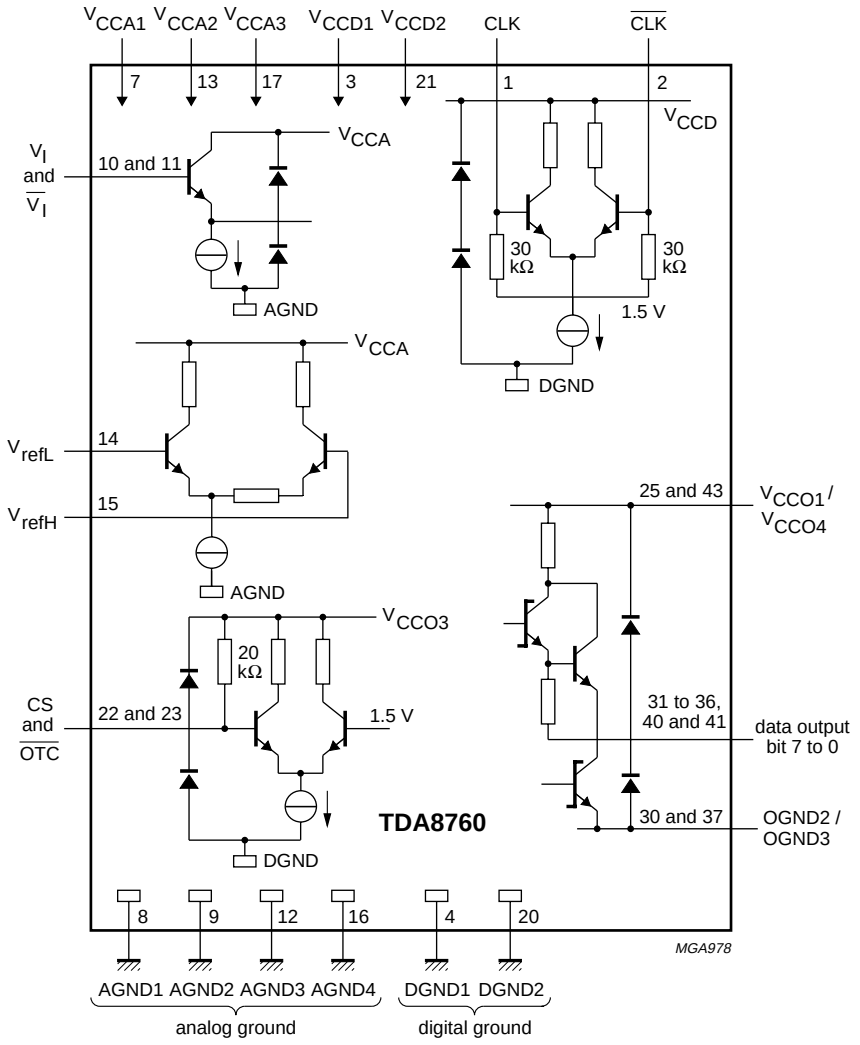
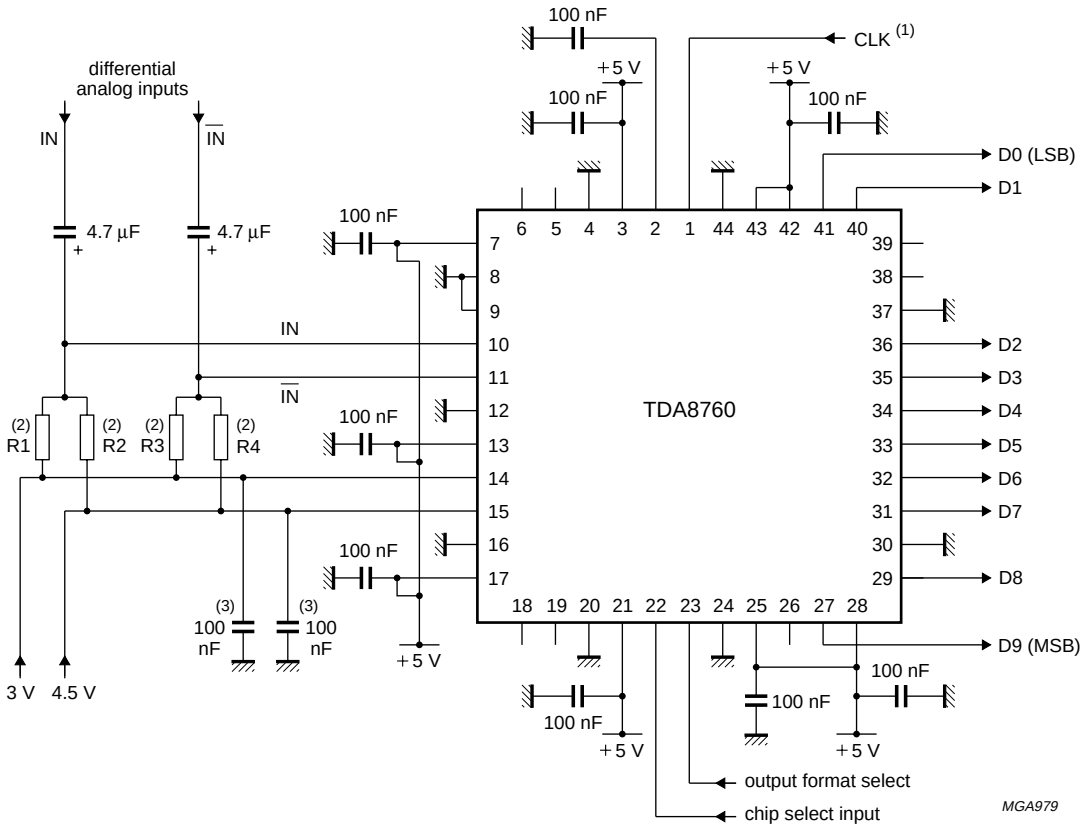



Fig.10 Description of input and output circuitry.

## APPLICATION INFORMATION



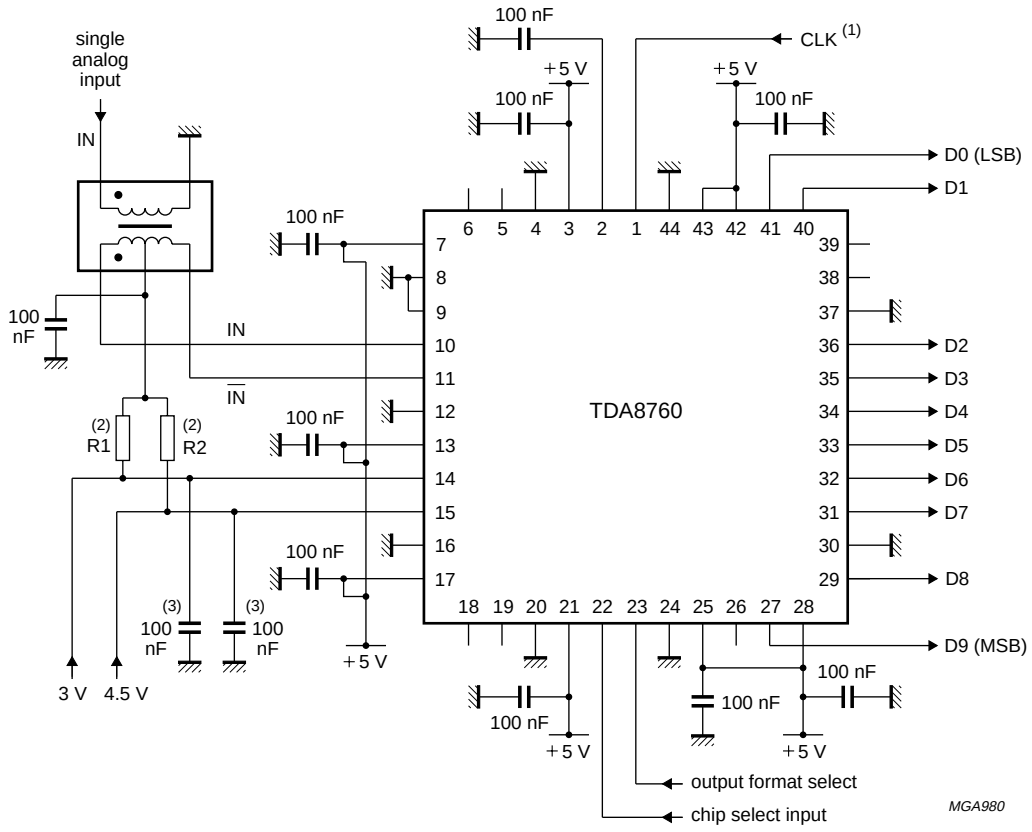

The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

(2) R1 and R2 must be determined in order to obtain a middle voltage of 3.4 V; see Table 1.

(3) $V_{refH}$ and $V_{refL}$ must be decoupled to AGND.

Fig.11 Application diagram for differential input mode.



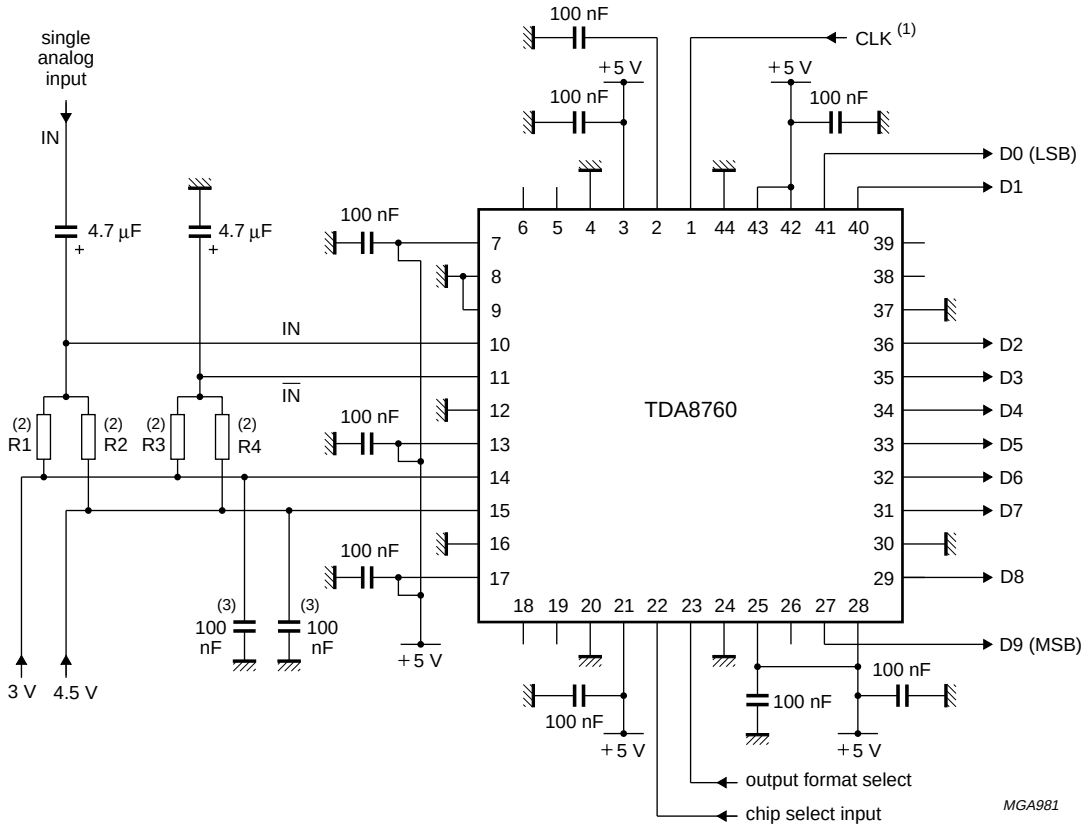

The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

(2) R1 and R2 must be determined in order to obtain 3.4 V at the transformer; see Table 1. Adaptation with the single input signal impedance must be taken care of.

(3) $V_{refH}$ and $V_{refL}$ must be decoupled to AGND.

Fig.12 Application diagram for differential input mode using an input transformer.




The analog, digital and output supplies should be separated and decoupled.

(1) Differential clock signals can be applied if required.

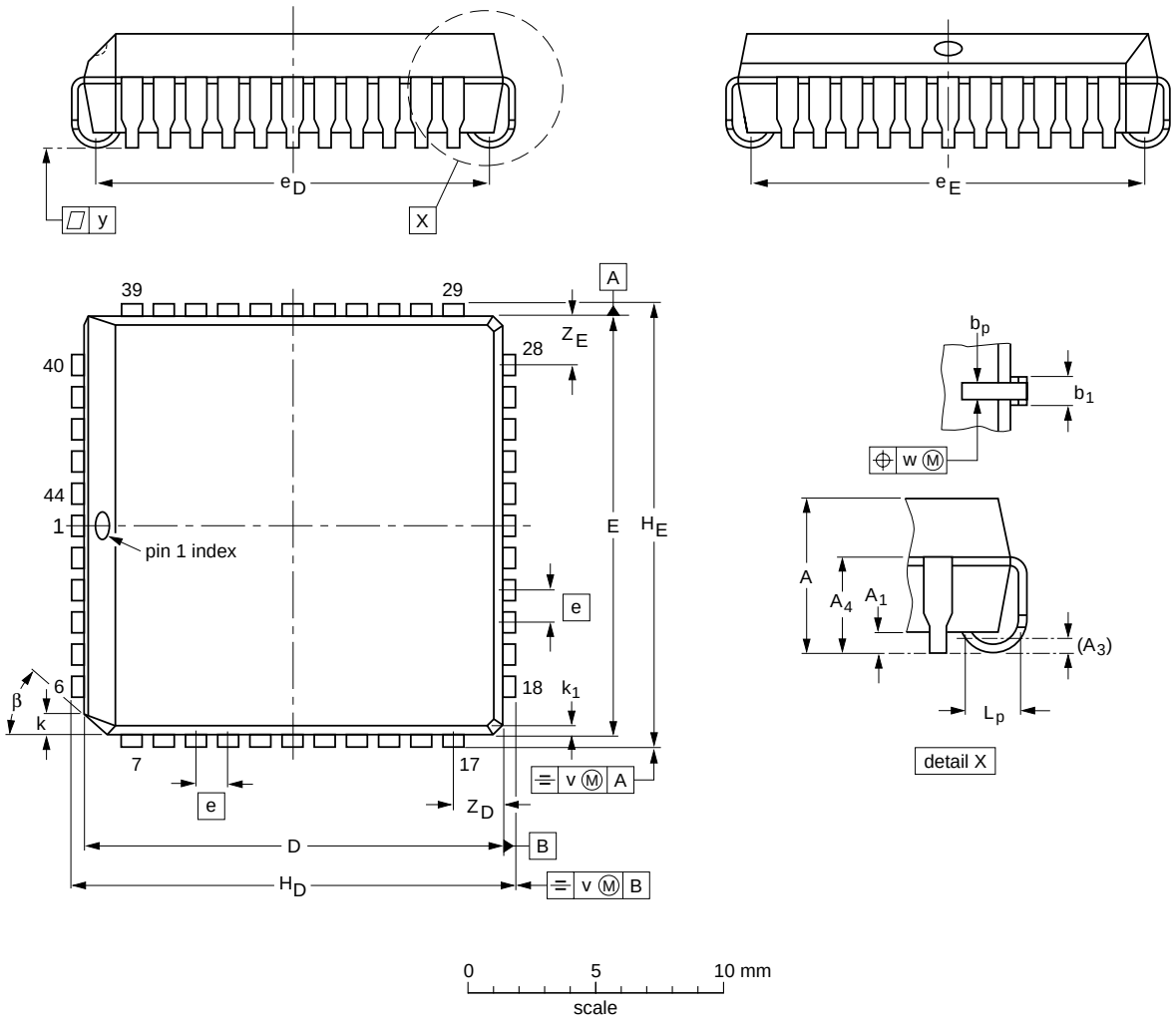
(2) R1 = R3; R2 = R4. R1, R2, R3 and R4 must be determined in order to obtain a middle voltage of 3.7 V; see Table 2.

(3) $V_{refH}$ and $V_{refL}$ must be decoupled to AGND.

Fig.13 Application diagram for single input mode.

## PACKAGE OUTLINE

**PLCC44: plastic leaded chip carrier; 44 leads** **SOT187-2**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | $D^{(1)}$ | $E^{(1)}$ | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $k_1$ max. | $L_p$ | v | w | y | $Z_D^{(1)}$ max. | $Z_E^{(1)}$ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 16.66<br>16.51 | 16.66<br>16.51 | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07 | 0.51 | 1.44<br>1.02 | 0.18 | 0.18 | 0.10 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.020 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650 | 0.656<br>0.650 | 0.05 | 0.630<br>0.590 | 0.630<br>0.590 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.020 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT187-2 | 112E10 | MO-047AC | | | | ~~95-02-25~~<br>97-12-16 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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